

Pixel change detection camera

8 sheets: this overview, then one sheet per function. Nets between sheets are global labels: power rails are power symbols.

USB-C power input and more

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- USB-C power input
 - 3.3 V buck converter
 - FPGA core supply (1.2 V)

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ESP32-S3-MINI-1-N8 (U9)

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Camera connector (OV5640) and more

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Camera supplies (2.8 V, 1.5 V)

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BOOT (SW1), RESET (SW2) and more

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ASM330LHH motion sensor (IMU)

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- ASM330LHH motion sensor (IMU)

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Power tree
VBUS (from J1)
-> F1 1.1A PTC -> +5V
-> U1 TLV62569DBVR -> +3V3
-> U4 ME6211C12M5G-N -> +1V2
-> R9 10R -> FPGA_VPLL
-> U3 ME6211C15M5G-N -> +1V5
-> U2 ME6211C28M5G-N -> +2V8
-> FB1 600R@100MHz -> CAM_AVDD

Generated from the netlist (run/state/circuit_graph.json) – do not edit by hand
Sheet: Overview
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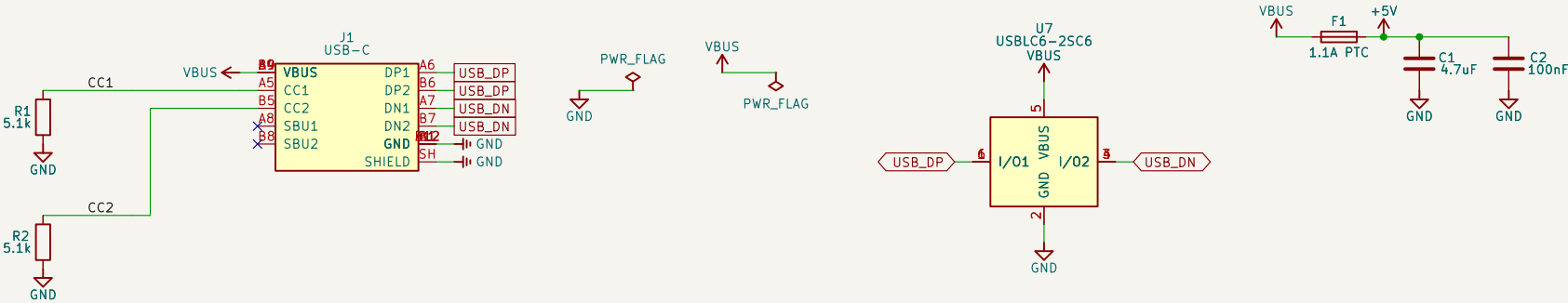
Sheet: /
File: board.kicad_sch

Title: Pixel change detection camera

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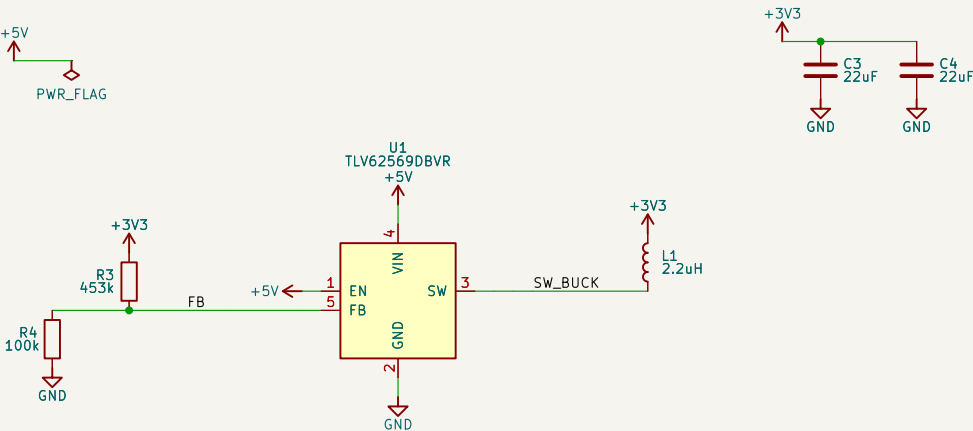
USB-C power input

The only power source. Plug a USB-C cable in and the whole board runs from its 5 V. The ESP32's USB lines are on this connector too (flashing, serial log). 5.1 kOhm pull-downs on CC1 / CC2 make the board a USB-C sink, so C-to-C and A-to-C cables both give 5 V. The 1.1 A resettable fuse protects the port; USBLC6-2SC6 clamps ESD on D+, D- and VBUS. Worst-case input is about 0.5 A (Wi-Fi transmit peaks), the limit of a plain USB 2.0 port – use a port or charger that can give 0.5 A or more. There is no coin cell and no battery backup; the board has no RTC backup domain.



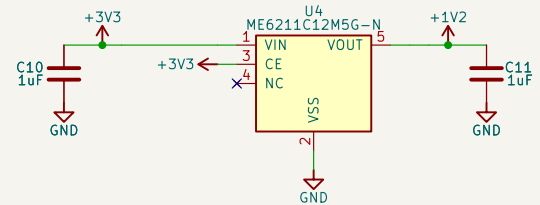
3.3 V buck converter

Turns the USB 5 V into the 3.3 V that the ESP32, the flash, the IMU and the FPGA's I/O run from. A switching regulator is used because Wi-Fi bursts are far too hungry for a simple linear one. TLV62569 (2 A) with a 2.2 uH inductor; the 453 k / 100 k feedback divider sets 3.32 V. Output capacitance 2 x 22 uF plus the 10 uF at the ESP32 and the IMU.



FPGA core supply (1.2 V)

A small regulator that makes the 1.2 V the FPGA's logic core runs from. ME6211 1.2 V version, fed from 3.3 V; the FPGA core takes tens of mA.



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Sheet: USB-C power input and more

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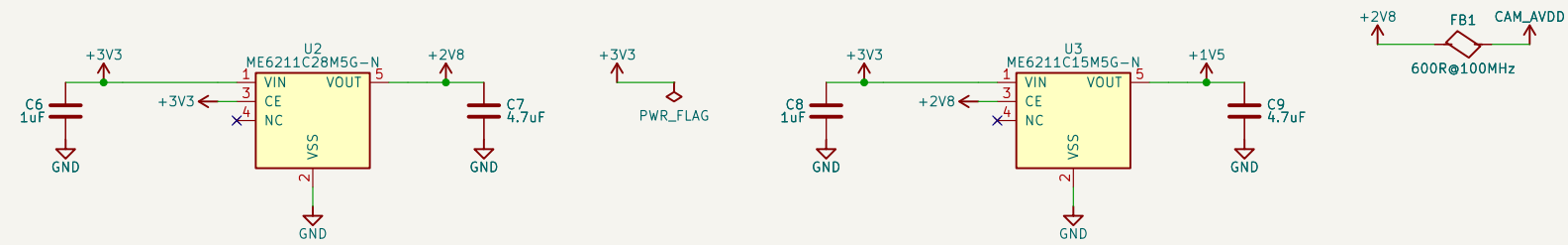
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Camera supplies (2.8 V, 1.5 V)

Two small regulators make the supplies the OV5640 camera needs – 2.8 V for its analog part and I/O, 1.5 V for its digital core.
The 1.5 V regulator is enabled by the 2.8 V rail, so the camera's digital core powers up after its I/O and analog supplies.
A ferrite bead (600 ohm at 100 MHz) separates the camera's analog supply (AVDD) from the noisy 2.8 V rail.
The 2.8 V rail also powers FPGA bank 0 (the camera signals), so the FPGA sees the camera's own logic levels.



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Sheet: Camera supplies (2.8 V, 1.5 V)

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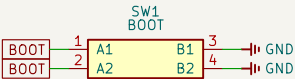
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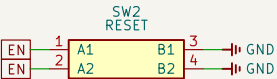
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BOOT (SW1)

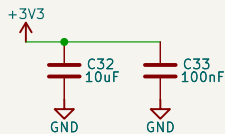
The ESP32-S3-MINI-1 does the Wi-Fi and runs the firmware. It reads the change results from the FPGA over SPI, configures the camera over I2C and talks to the IMU. The antenna end of the module hangs over the top edge of the board – keep metal and your hand away from it. BOOT button (GPIO0) held while pressing RESET starts the USB download mode; the chip's built-in USB is wired to the USB-C connector, so no separate USB-serial chip is needed. Pins used – FPGA link: GPIO10 CS, 11 MOSI, 12 SCK, 13 MISO, 14 IRQ, 15 CRESET_B, 16 CDONE; camera SCCB: GPIO38 SDA, 39 SCL, 40 RESET; IMU: GPIO8 SDA, 9 SCL, 7 INT1, 6 INT2; user LED GPIO21. UART0 TX / RX (GPIO43 / 44) are on two test pads for the boot log.



RESET (SW2)



ESP32-S3-MINI-1-N8 (U9): decoupling



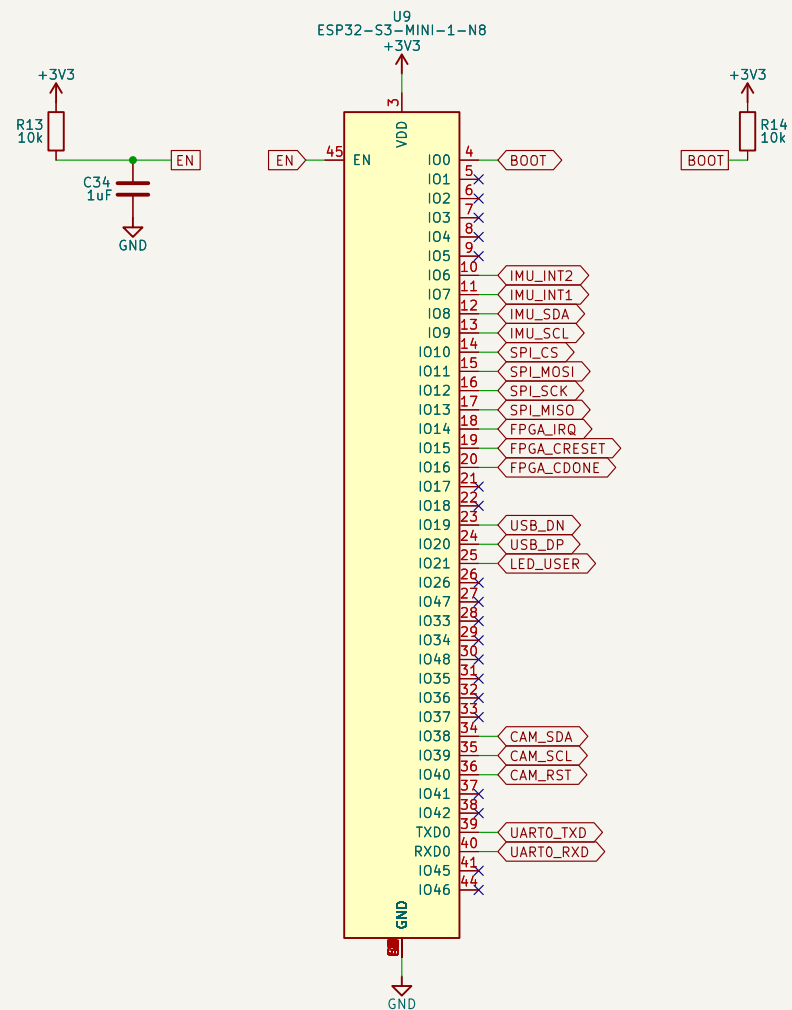
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Sheet: BOOT (SW1), RESET (SW2) and more

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Sheet: /BOOT (SW1), RESET (SW2) and more/
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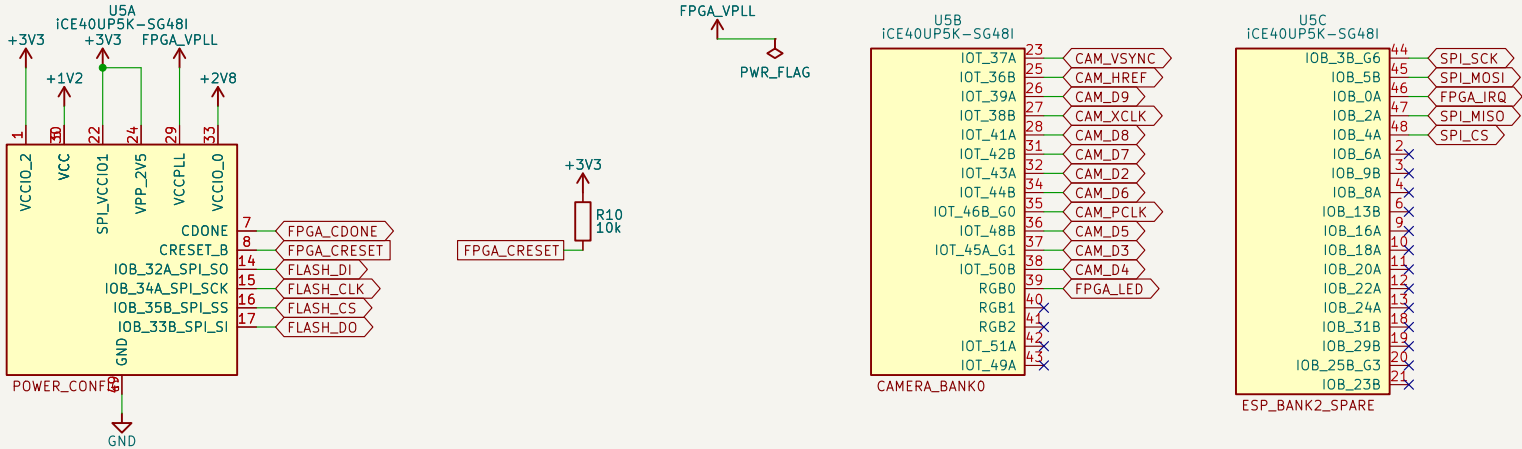
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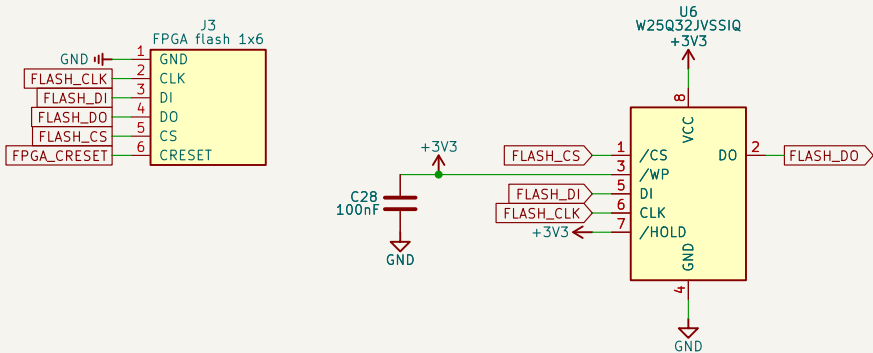
ice40 FPGA (change detection)

The Lattice iCE40UP5K takes the camera's pixel stream, keeps one reference frame in its on-chip RAM and flags the pixels that changed. It passes the result to the ESP32. Bank 0 (camera side) runs at 2.8 V, banks 1 and 2 (flash and ESP32 side) at 3.3 V; VCC and VCCPLL are 1.2 V (VCCPLL through 10 ohm and 100 nF). 1 Mbit of SPRAM holds one QVGA (320 x 240) 8-bit reference frame (76.8 kB); set the camera to a low resolution YUV mode and use only the Y byte. The FPGA loads its design from the SPI flash after power-up; CRESET_B has a 10 k pull-up and the ESP32 can hold it low to restart configuration; CDONE tells the ESP32 it is configured. The ESP32 link is SPI (ESP32 is master) plus an interrupt line; the camera data bits may be reordered inside the FPGA design. The red LED on the FPGA's open-drain RGB0 pin is free for the design.



FPGA configuration flash

A 32 Mbit SPI flash that holds the FPGA's design. The 6-pin header lets you write it with an external SPI programmer. Header pins: 1 GND, 2 CLK, 3 DI, 4 DO, 5 CS, 6 CRESET_B. To program, power the board by USB, hold CRESET_B low (header pin 6 to GND) so the FPGA lets go of the bus, then write the flash (3.3 V logic). The flash's /WP and /HOLD are tied to 3.3 V, so only single-bit SPI is used.



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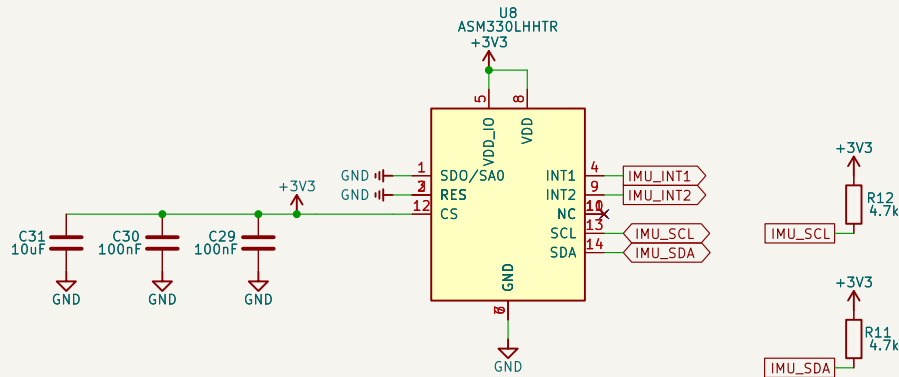
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ASM330LHH motion sensor (IMU)

ST's automotive-grade 6-axis sensor (3-axis accelerometer and 3-axis gyroscope) on the I2C bus.
I2C address 0x6A (SDO / SA0 tied to GND); CS is tied high to select I2C. Interrupt outputs go to GPIO7 and GPIO6.



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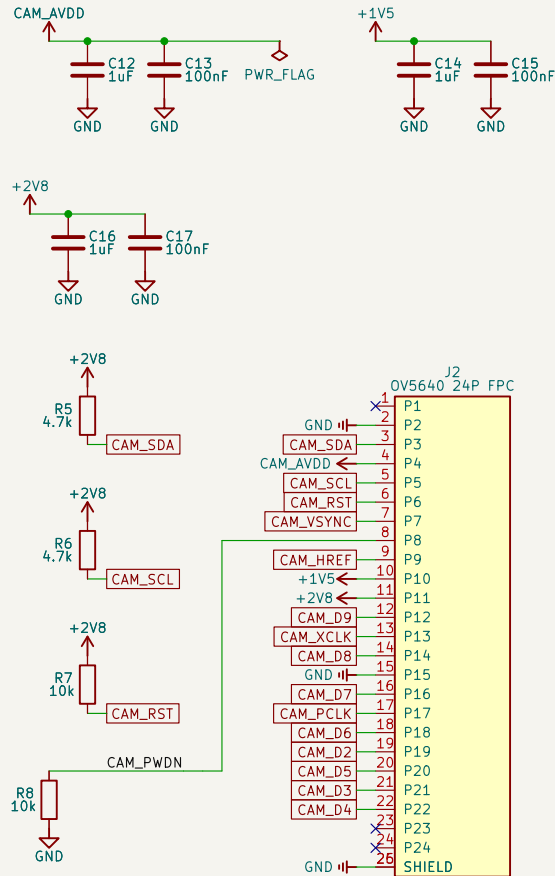
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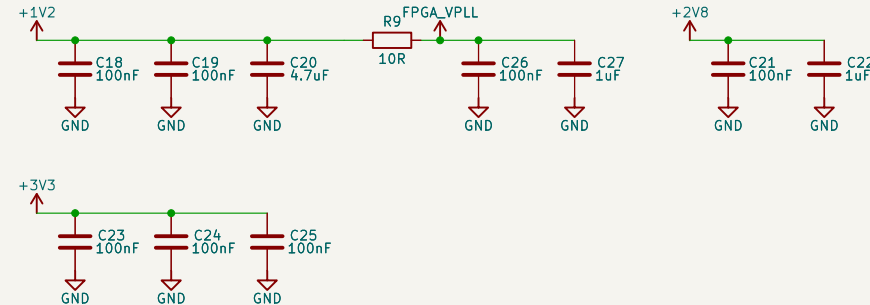
Camera connector (OV5640)

A 24-pin 0.5 mm flat-cable socket for an OV5640 camera module with a parallel (DVP) interface.
Pin order (module side): 1 NC, 2 AGND, 3 SDA, 4 AVDD, 5 SCL, 6 RESET, 7 VSYNC, 8 PWDN, 9 HREF, 10 DVDD, 11 DOVDD, 12 D9, 13 XCLK, 14 D8, 15 GND, 16 D7, 17 PCLK, 18 D6, 19 D2, 20 D5, 21 D3, 22 D4, 23-24 NC.
Check your module's pin list and which side of its flex carries the contacts before you plug it in - 24-pin OV5640 modules from different makers are not all wired alike.
SDA / SCL have 4.7 k pull-ups to 2.8 V and are driven by the ESP32 (open drain); RESET is pulled up to 2.8 V and PWDN pulled low (camera always on). The FPGA makes the 24 MHz clock for the camera (XCLK).
Supply budget through the connector - AVDD 40 mA, DVDD 80 mA, DOVDD 20 mA.



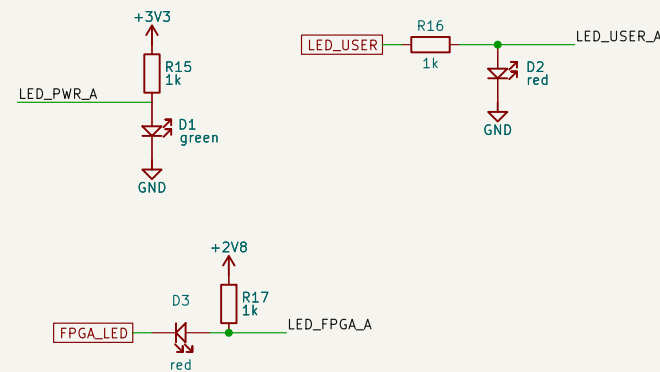
FPGA decoupling

Small capacitors right at the FPGA's supply pins that keep its supplies steady.
VCC (1.2 V) has 100 nF at each of its two pins plus 4.7 uF; the PLL supply goes through 10 ohm and 100 nF + 1 uF.



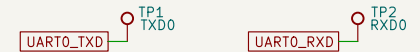
Status LEDs

A green power light, a red light the firmware can use on the ESP32 and a red light for the FPGA design.
The red LED is on GPIO21 through 1 kOhm.



UART test pads

Two pads for the ESP32's serial boot log (TX and RX of UART0).



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